

400MHz Wideband AGC Amplifier

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The SL6140 is an integrated broadband AGC amplifier, designed on an advanced bipolar process. The amplifier provides over 15dB of linear gain into 50 at 400MHz. Gain control is also provided with over 70dB of dynamic range. The SL6140 offers over 45dB of voltage gain with an R₁ of 1k .

FEATURES

- 400MHz Bandwidth (R $_{\rm L}$ =50) High voltage Gain 45dB (R $_{\rm L}$ =1k)
- 70dB Gain Control Range
- High Output Level at Low Gain
- Surface Mount Plastic Package
- Low Cost

APPLICATIONS

- RF/IF Amplifier
- High Gain Mixers
- Video Amplifiers

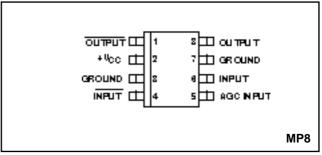


Fig.1 Pin connections top view

ORDERING INFORMATION

SL6140/NA/MP Industrial temperature range miniature plastic package.

SL6140/NA/MPTC Tape and Reel

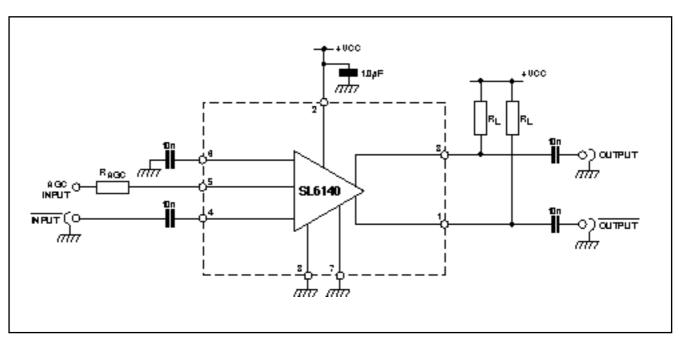


Fig.2 Typical application

SL6140

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated)

 $\mathsf{T}_{\mathsf{amb}} = 25^{\circ}\mathsf{C},\, \mathsf{V}_{\mathsf{CC}} = 12\mathsf{V} + 5\%,\, \mathsf{V}_{\mathsf{IN}} = 1\mathsf{m}\mathsf{V}_{\mathsf{RMS}},\, \mathsf{Frequency} = 6\mathsf{MHz},\, \mathsf{Load}\,(\mathsf{R}_{\mathsf{L}}) = 10\mathsf{KOHms},\, \mathsf{R}_{\mathsf{AGC}} = 22\mathsf{KOHm}$

Characteristic	Pin	Value			Unita	Conditions
Characteristic		Min	Тур	Max	Units	Conditions
Supply current	5,6,7		19	23	mA	No input signal
Output stage current	5,6 (sum)	5	7	9	mA	No input signal
Output current matching (magnitude of difference of output currents)	5,6		1.0		mA	See Note 2
AGC range	2	60	75		dB	See Fig. 4 & Note 1 (VAGC = 0V to 10V)
Voltage gain (single ended)	5,6	40	45 55		dB dB	R _L = 1k See Fig. 5 & Note 1 Tuned input and output
	5,6		15		dB	R _L = 50
Bandwidth (-3dB)	5,6		25 400		MHz	RL = 1k See Fig. 5. See Note 2 RL = 50
Maximum output level (single ended)						
0dB AGC	5,6		3.5		V p-p	Note 1
-30dB AGC	5,6		3.5		V p-p	R _L = 1k . Note 1
Noise figure	5,6		5		dB	Test CCT Fig. 13

Note. 1 Guaranteed but not tested.

DESCRIPTION

The SL6140 (Fig. 3) is a high gain amplifier with an AGC control capable of reducing the gain of the amplifier by over 70dB. The gain is adjustable by applying a voltage to the AGC input via an external resistor ($R_{\rm AGC}$), the value of which adjusts the curve of gain reduction versus control voltage (see Fig. 4). As the output stage of the amplifier is an open collector the maximum voltage gain is determined by $R_{\rm L}$. With load resistance of 1k $\,$ the single ended voltage gain is 45dB and with a load resistance of 50 $\,$ the voltage gain is 15dB (20log $_{10}$ V $_{\rm OUT}$ /V $_{\rm IN}$). Another parameter that depends on the load resistance is the bandwidth: 25MHz for $R_{\rm L}$ = 1k $\,$, as compared with 400MHz for $R_{\rm L}$ = 50 $\,$. $R_{\rm L}$ is chosen to give either the required bandwidth or voltage gain for the circuit.

Figs. 7 through to 10 show the typical S parameters for the device. Figs. 11 and 12 show the typical variation in 3rd order intercept performance with AGC.

In any application, the substrate should be connected to the most negative point in the circuit, usually to the same point as pin 3.

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V _{CC}	+18V
Input voltage (differential)	+5V
AGC supply	V_{CC}
Storage temperature	-55°C to +150°C
Operating temperature range	
SL6140 MP	-40°C to +85°C
	at 200mW
Chip operating temperature	
SL6140 MP	+150°C

THERMAL RESISTANCE

Chip-to-ambient	
SL6140 MP	163°C/W
Chip-to-case	
SL6140 MP	57°C/W

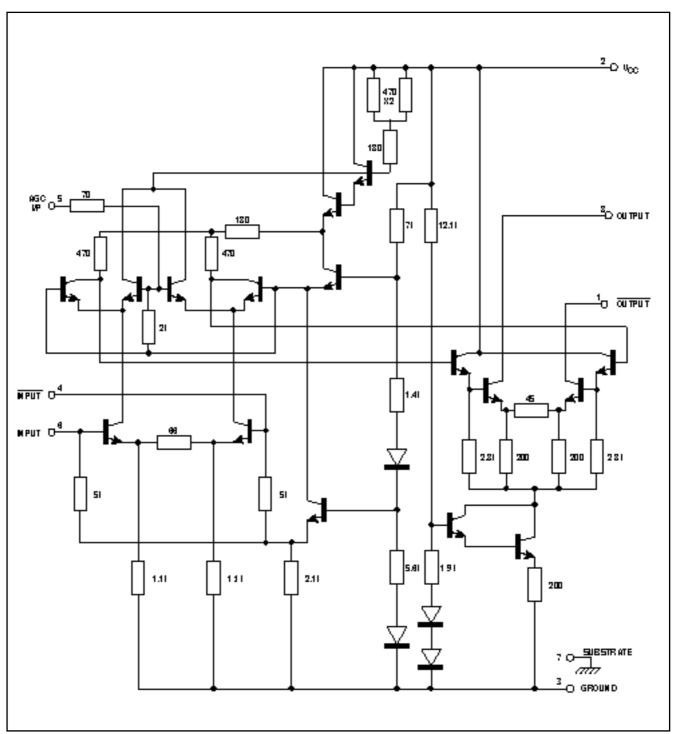


Fig. 3 Full circuit diagram of SL6140

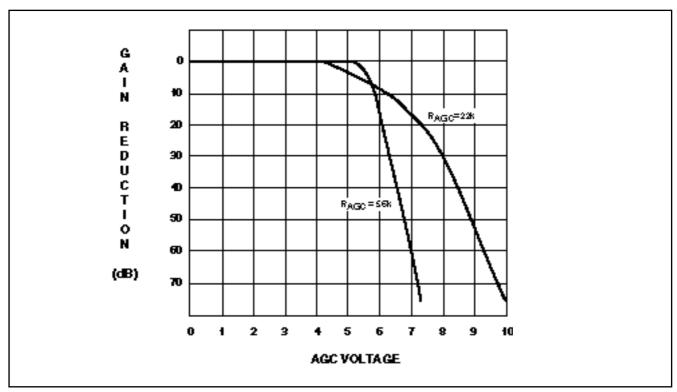


Fig. 4 Gain reduction v. AGC voltage

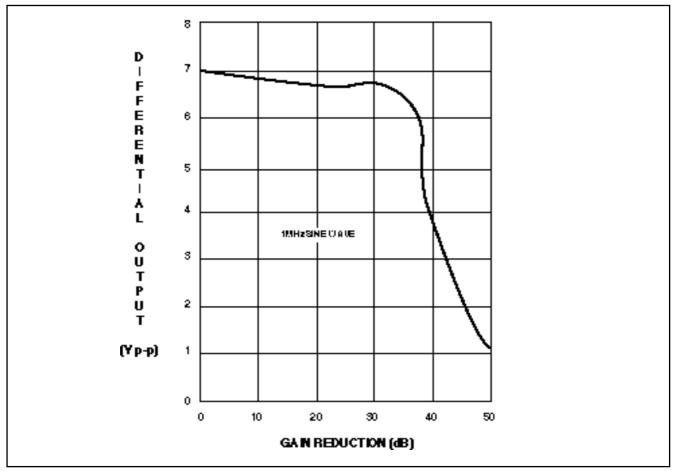


Fig. 5 Max differential O/P voltage v. gain reduction

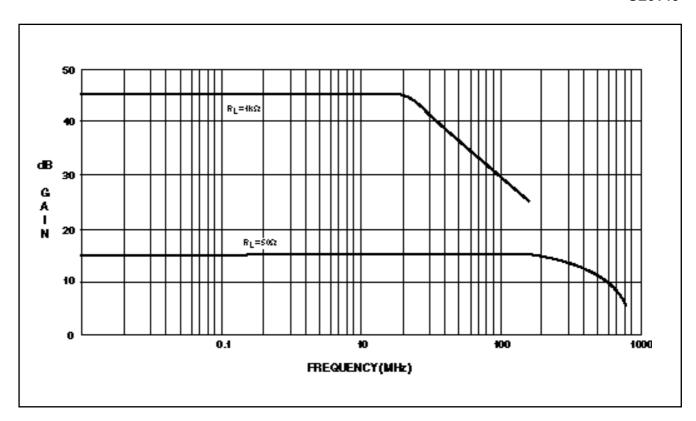


Fig. 6 Voltage Gain v. Frequency

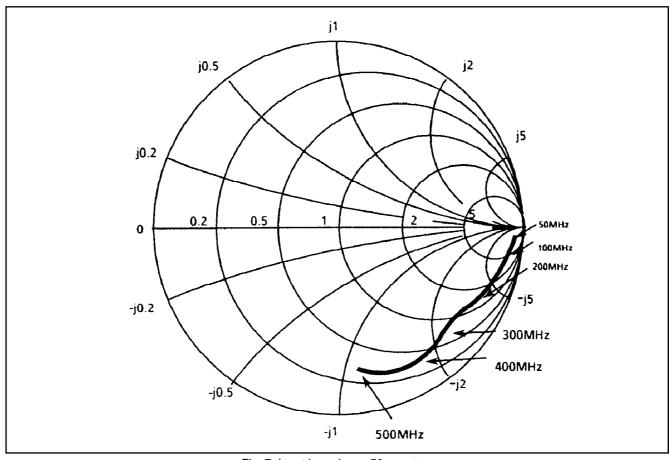


Fig. 7 Input impedance 50 system

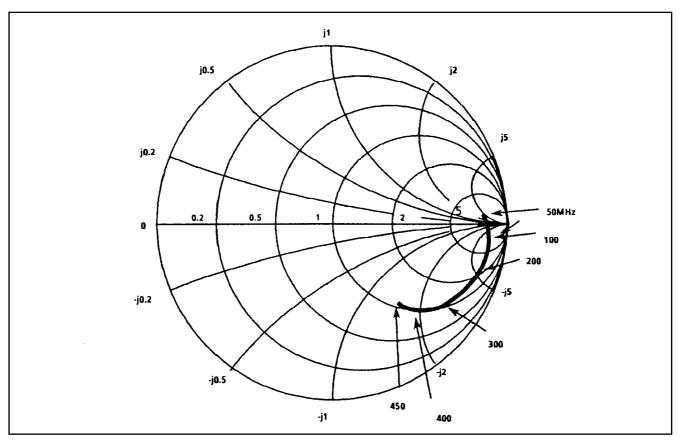


Fig. 8 Output impedance 50 system

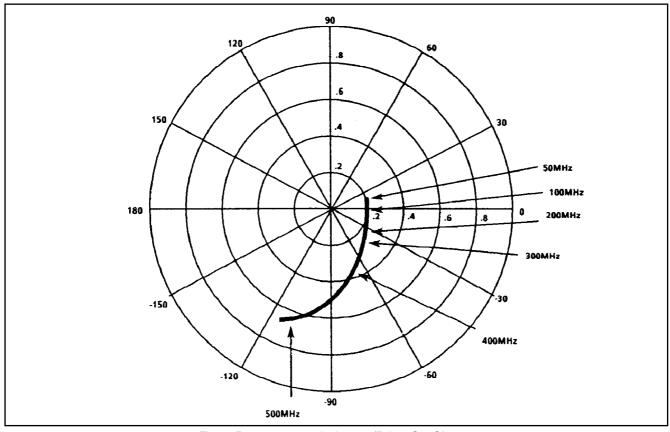


Fig. 9 Reverse transmission coefficient S_{12} SL6140

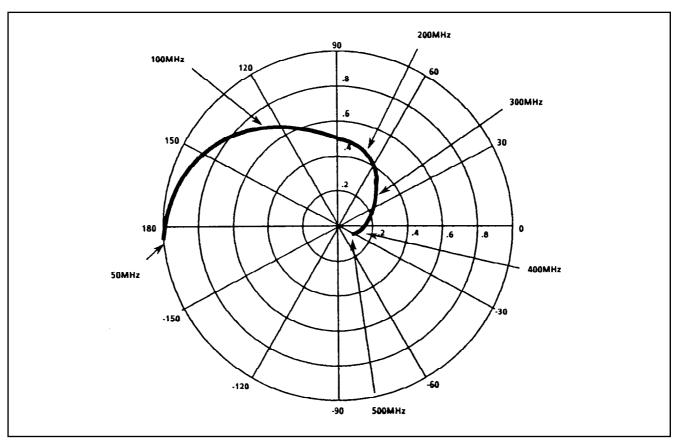


Fig. 10 Forward transmission coefficients S_{21} SL6140

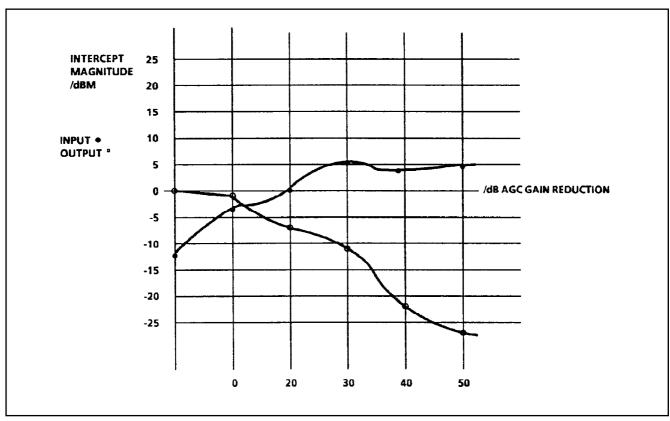


Fig. 11 3rd Order intercept point against gain reduction at 250.0MHz and 254.0MHz

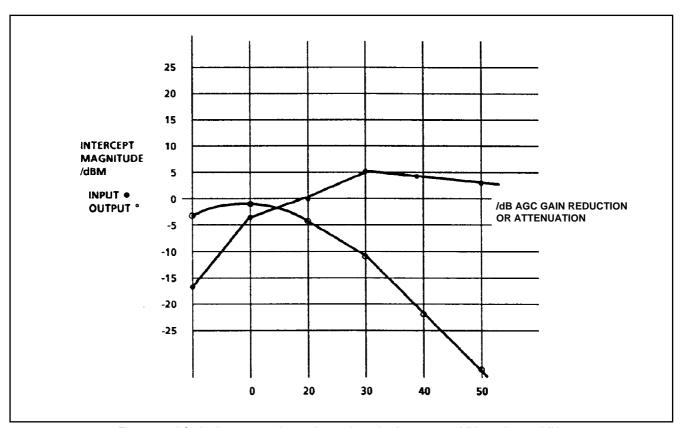


Fig. 12 3rd Order intercept point against gain reduction at 100.0MHz and 104.0MHz

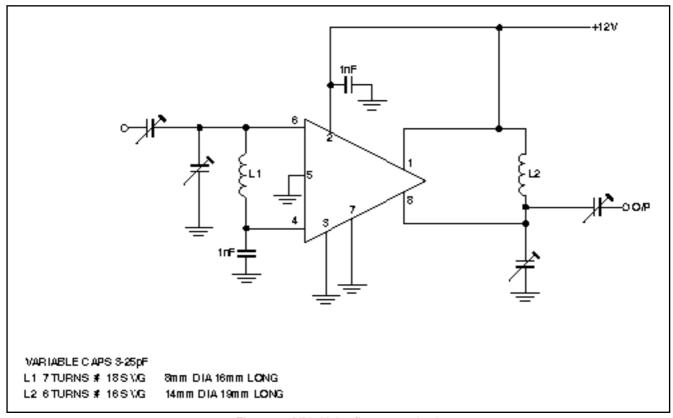


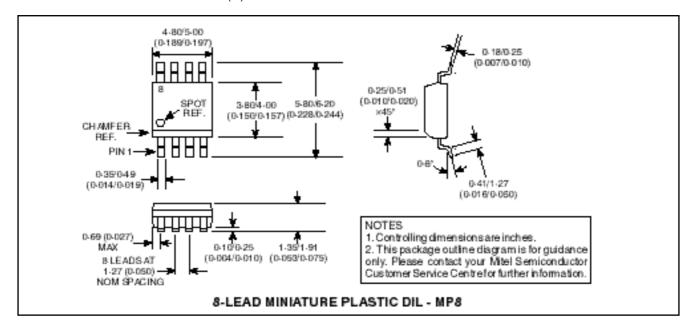
Fig. 13 50MHz Noise figure test circuit

SL6140

SL6140

PACKAGE DETAILS

Dimensions are shown thus: mm (in).





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